

**WHAT IS CLAIMED IS:**

1       1. A data processor comprising:

2                 an instruction execution pipeline comprising N processing  
3                 stages; and

4                 an instruction issue unit capable of fetching into said  
5                 instruction execution pipeline instructions fetched from an  
6                 instruction cache associated with said data processor, each of said  
7                 fetched instructions comprising from one to S syllables, said  
8                 instruction issue unit comprising;

9                 a first buffer comprising S storage locations  
10                capable of receiving and storing said one to S syllables  
11                associated with said fetched instructions, each of said S  
12                storage locations capable of storing one of said one to S  
13                syllables of each fetched instruction;

14                a second buffer comprising S storage locations  
15                capable of receiving and storing said one to S syllables  
16                associated with said fetched instructions, each of said S  
17                storage locations capable of storing one of said one to S  
18                syllables of each fetched instruction; and

19                a controller capable of determining if a first one  
20                of said S storage locations in said first buffer is full,  
21                wherein said controller, in response to a determination that

22        said first one of said S storage locations is full, causes a  
23        corresponding syllable in an incoming fetched instruction to  
24        be stored in a corresponding one of said S storage locations  
25        in said second buffer.

1            2.        The data processor as set forth in Claim 1 wherein S=4.

1            3.        The data processor as set forth in Claim 1 wherein S=8.

1            4.        The data processor as set forth in Claim 1 wherein S is  
a multiple of four.

1            5.        The data processor as set forth in Claim 1 wherein each  
of said one to S syllables comprises 32 bits.

1            6.        The data processor as set forth in Claim 1 wherein each  
2        of said one to S syllables comprises 16 bits.

1            7.        The data processor as set forth in Claim 1 wherein each  
2        of said one to S syllables comprises 64 bits.

1       8. The data processor as set forth in Claim 1 wherein said  
2 controller is capable of determining when all of the syllables in  
3 one of said fetched instructions are present in said first buffer,  
4 wherein said controller, in response to a determination that said  
5 all of said syllables are present, causes said all of said  
6 syllables to be transferred from said first buffer to said  
7 instruction execution pipeline.

1       9. The data processor as set forth in Claim 8 wherein said  
2 controller is capable of determining if a syllable in said first  
3 one of said S storage locations in said first buffer has been  
4 transferred from said first buffer to said instruction pipeline,  
5 wherein said controller, in response to a determination that said  
6 first one of said S storage locations has been transferred, causes  
7 said corresponding syllable stored in said corresponding one of  
8 said S storage locations in said second buffer to be transferred to  
9 said first one of said S storage locations in said first buffer.

1           10. The data processor as set forth in Claim 9 further  
2 comprising a switching circuit controlled by said controller and  
3 operable to transfer syllables from said second buffer to said  
4 first buffer.

1           11. A processing system comprising:  
2            a data processor;  
3            a memory coupled to said data processor;  
4            a plurality of memory-mapped peripheral circuits coupled  
5        to said data processor for performing selected functions in  
6        association with said data processor, wherein said data processor  
7        comprises:

8                  an instruction execution pipeline comprising N  
9        processing stages; and

10                 an instruction issue unit capable of fetching into  
11        said instruction execution pipeline instructions fetched from  
12        an instruction cache associated with said data processor, each  
13        of said fetched instructions comprising from one to S  
14        syllables, said instruction issue unit comprising;

15                 a first buffer comprising S storage locations  
16        capable of receiving and storing said one to S syllables  
17        associated with said fetched instructions, each of said  
18        S storage locations capable of storing one of said one to  
19        S syllables of each fetched instruction;

20                 a second buffer comprising S storage locations  
21        capable of receiving and storing said one to S syllables  
22        associated with said fetched instructions, each of said

23           S storage locations capable of storing one of said one to  
24           S syllables of each fetched instruction; and  
25                    a controller capable of determining if a first  
26           one of said S storage locations in said first buffer is  
27           full, wherein said controller, in response to a  
28           determination that said first one of said S storage  
29           locations is full, causes a corresponding syllable in an  
30           incoming fetched instruction to be stored in a  
corresponding one of said S storage locations in said  
second buffer.

12. The processing system as set forth in Claim 11 wherein

S=4 .

13. The processing system as set forth in Claim 11 wherein

S=8 .

1           14. The processing system as set forth in Claim 11 wherein S

2           is a multiple of four.

1           15. The processing system as set forth in Claim 11 wherein  
2    each of said one to S syllables comprises 32 bits.

1           16. The processing system as set forth in Claim 11 wherein  
2    each of said one to S syllables comprises 16 bits.

1           17. The processing system as set forth in Claim 11 wherein  
2    each of said one to S syllables comprises 64 bits.

1           18. The processing system as set forth in Claim 11 wherein  
2    said controller is capable of determining when all of the syllables  
3    in one of said fetched instructions are present in said first  
4    buffer, wherein said controller, in response to a determination  
5    that said all of said syllables are present, causes said all of  
6    said syllables to be transferred from said first buffer to said  
7    instruction execution pipeline.

1           19. The processing system as set forth in Claim 18 wherein  
2       said controller is capable of determining if a syllable in said  
3       first one of said S storage locations in said first buffer has been  
4       transferred from said first buffer to said instruction pipeline,  
5       wherein said controller, in response to a determination that said  
6       first one of said S storage locations has been transferred, causes  
7       said corresponding syllable stored in said corresponding one of  
8       said S storage locations in said second buffer to be transferred to  
      said first one of said S storage locations in said first buffer.

2           20. The processing system as set forth in Claim 19 further  
3       comprising a switching circuit controlled by said controller and  
4       operable to transfer syllables from said second buffer to said  
      first buffer.

1           21. For use in a data processor comprising an instruction  
2 execution pipeline comprising N processing stages, a method of  
3 fetching into the instruction execution pipeline instructions  
4 fetched from an instruction cache associated with the data  
5 processor, each of the fetched instructions comprising from one to  
6 S syllables, the method of fetching comprising the steps of:

7                 storing in a first buffer comprising S storage locations  
8 the one to S syllables associated with the fetched instructions,  
9 each of the S storage locations capable of storing one of the one  
10 to S syllables of each fetched instruction;

11                 determining if a first one of the S storage locations in  
12 the first buffer is full; and

13                 in response to a determination that the first one of the  
14 S storage locations is full, storing a corresponding syllable in an  
15 incoming fetched instruction in a corresponding one of S storage  
16 locations in a second buffer, wherein the second buffer comprises  
17 S storage locations, each of the S storage locations in the second  
18 buffer capable of storing one of the one to S syllables of each  
19 fetched instruction.

1           22. The method as set forth in Claim 21 wherein S is a  
2 multiple of four.

1           23. The method as set forth in Claim 21 wherein each of the  
2 one to S syllables comprises one of: a) 16 bits, b) 32 bits, and  
3 c) 64 bits.

1           24. The method as set forth in Claim 21 further comprising  
the steps of:

       determining when all of the syllables in one of the  
fetched instructions are present in the first buffer; and

       in response to a determination that all of the syllables  
are present, transferring all of the syllables from the first  
buffer to the instruction execution pipeline.

1           25. The method as set forth in Claim 24 further comprising  
2       the steps of:

3                   determining if a syllable in the first one of the S  
4       storage locations in the first buffer has been transferred from the  
5       first buffer to the instruction pipeline; and

6                   in response to a determination that the first one of the S  
7       S storage locations has been transferred, transferring the  
8       corresponding syllable stored in the corresponding one of the S  
     storage locations in the second buffer to the first one of the S  
     storage locations in the first buffer.